Bipolar junction Transistor

By

Assistant lecturer. Ahmed Saad Names

Text boxes

1. “Electronic Devices and Circuit Theory” Eleventh Edition, Robert L. Boylestad Louis Nashelsky, 2011

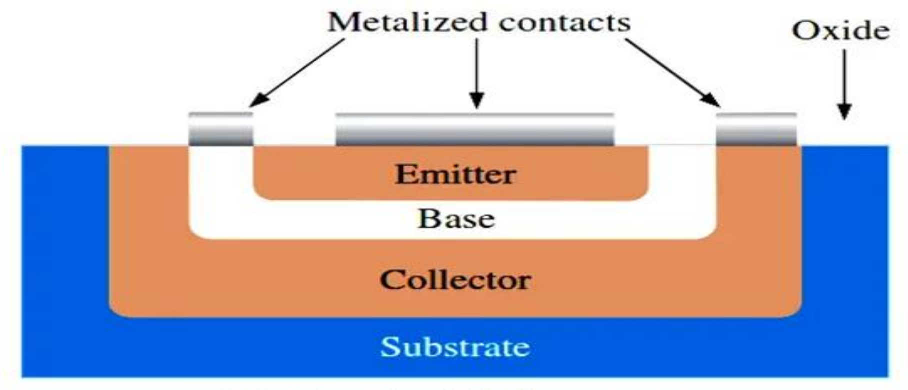
2. “Electronic Devices Electron Flow Version” Ninth Edition, Thomas L. Floyd, 2012

Transistor

- Three terminal active device which transforms current flow from low resistance path to high resistance path. This transfer of current through resistance path, given the name to the device '*transfer resistor*' as **transistor**.

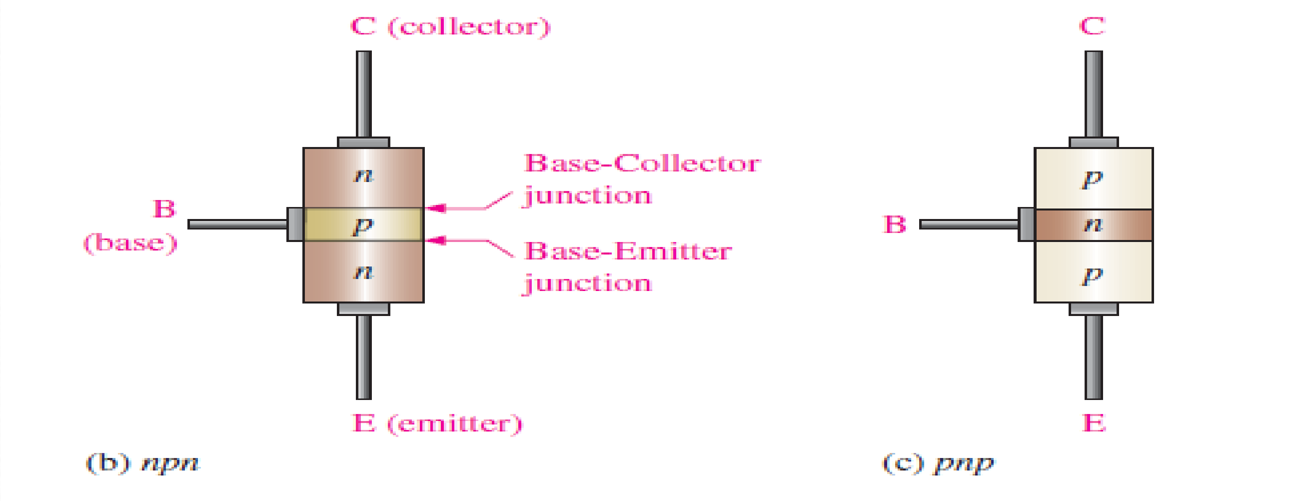
BJT

The BJT is constructed with three doped semiconductor regions separated by two *pn* junctions, as shown in the epitaxial planar structure in Figure (a). The three regions are called emitter, base, and collector. Physical representations of the two types of BJTs are shown in Figures (b) and (c).

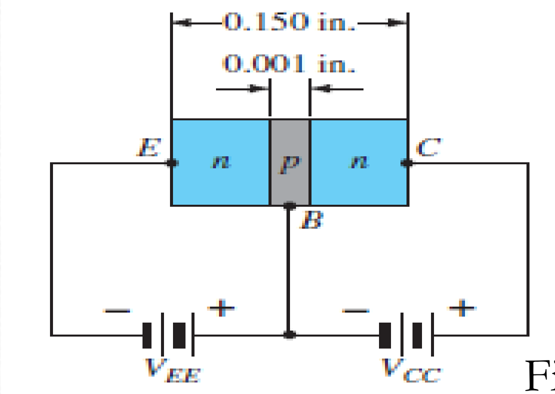


(a) Basic epitaxial planar structure

One type consists of two *n* regions separated by a *p* region (*npn*), and the other type consists of two *p* regions separated by an *n* region (*pnp*). The term **bipolar** refers to the use of both holes and electrons as current carriers in the transistor structure.



The outer layers have widths much greater than the sandwiched *p* - or *n* -type material. For the transistors shown in Figure (d) the ratio of the total width to that of the center layer is 0.1500.001 150:1. The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 1:10 or less).



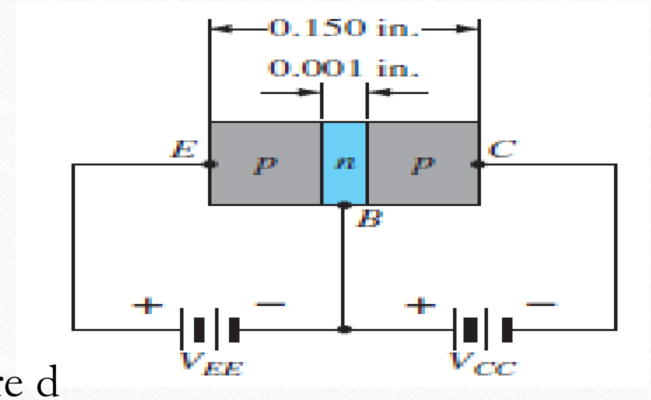
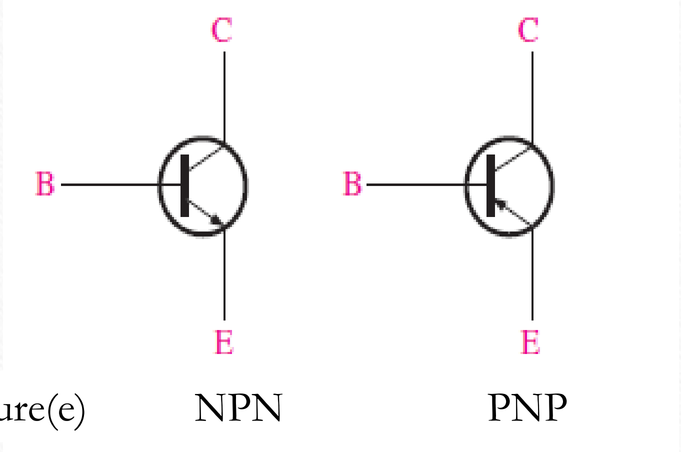


Figure d

The pn junction joining the base region and the emitter region is called the base-emitter junction. The pn junction joining the base region and the collector region is called the base-collector junction, These leads are labelled E, B, and C for emitter, base, and collector, respectively.

The base region is lightly doped and very thin compared to the heavily doped emitter and the moderately doped collector regions. Figure (e) shows the schematic symbols for the *npn* and *pnp* bipolar junction transistors



Figure(e)

BJT Modes Of Operation

- There are two junctions in bipolar junction transistor.
- Each junction can be forward or reverse biased independently.
- Thus there are different modes of operations:
- Forward Active. Cut off. Saturation.

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

FORWARD ACTIVE

- Emitter-base junction is forward biased and collector-base junction is reverse biased.
- The BJT can be used as an amplifier and in analog circuits.

CUTT OFF

- When both junctions are reverse biased it is called cut off mode.
- In this situation there is nearly zero current and transistor behaves as an open switch.

SATURATION

- In saturation mode both junctions are forward biased.
- Large collector current flows with a small voltage across collector base junction.
- Transistor behaves as an closed switch

Operation of pnp transistor in active mode

- The basic operation of the transistor will now be described using the *pnp* transistor.

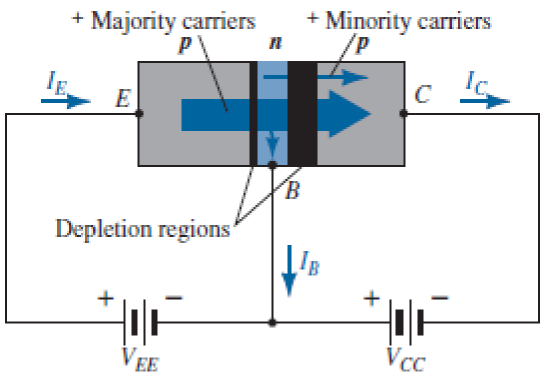
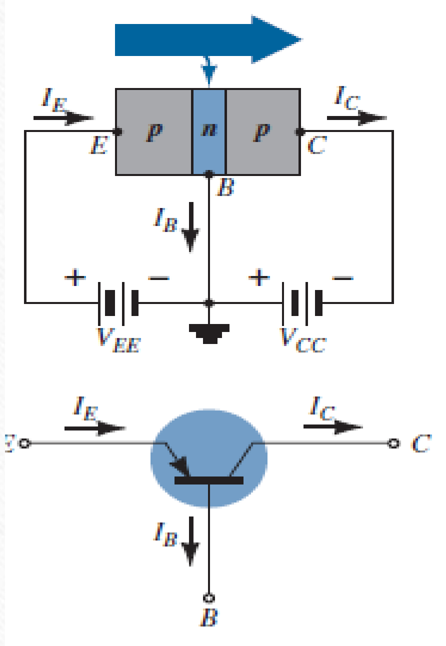


FIG. 5
Majority and minority carrier flow of a pnp transistor.

Currents in a Transistor

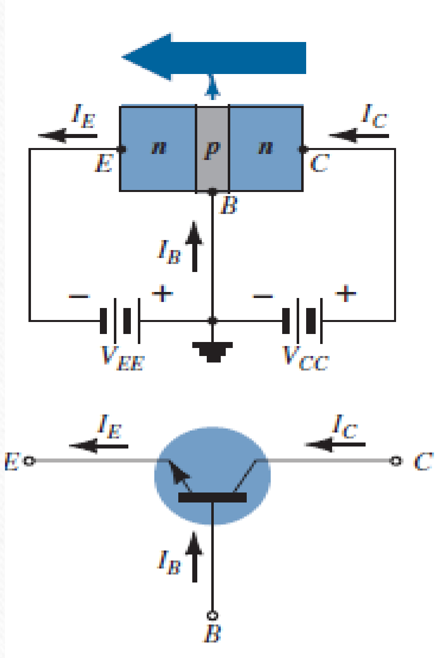
- Emitter current is the sum of the collector and base currents
- IE=IB+IC
- The collector current is comprised of two currents:
- IC=ICmajority +ICO minority
- The minority current is called the leakage current and is given by
- the symbol ICO (IC current with emitter terminal Open).

Common-base Configuration



(a)

The base is common to both input (emitter–base) and output (collector–base) of the transistor.



(b)

Common-Base Configuration

- The input set for the common-base amplifier as shown in Fig. 7 relates an input current (IE) to an input voltage (VBE) for various levels of output voltage (VCB).

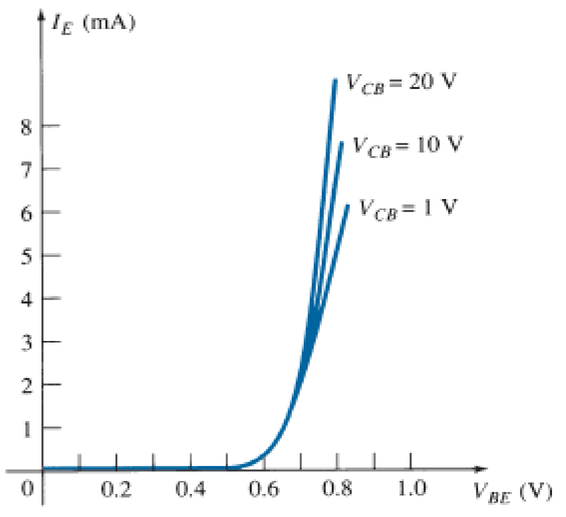


FIG. 7

- The output set relates an output current (IC) to an output voltage (VCB) for various levels of input current (IE) as shown in Fig. 8.

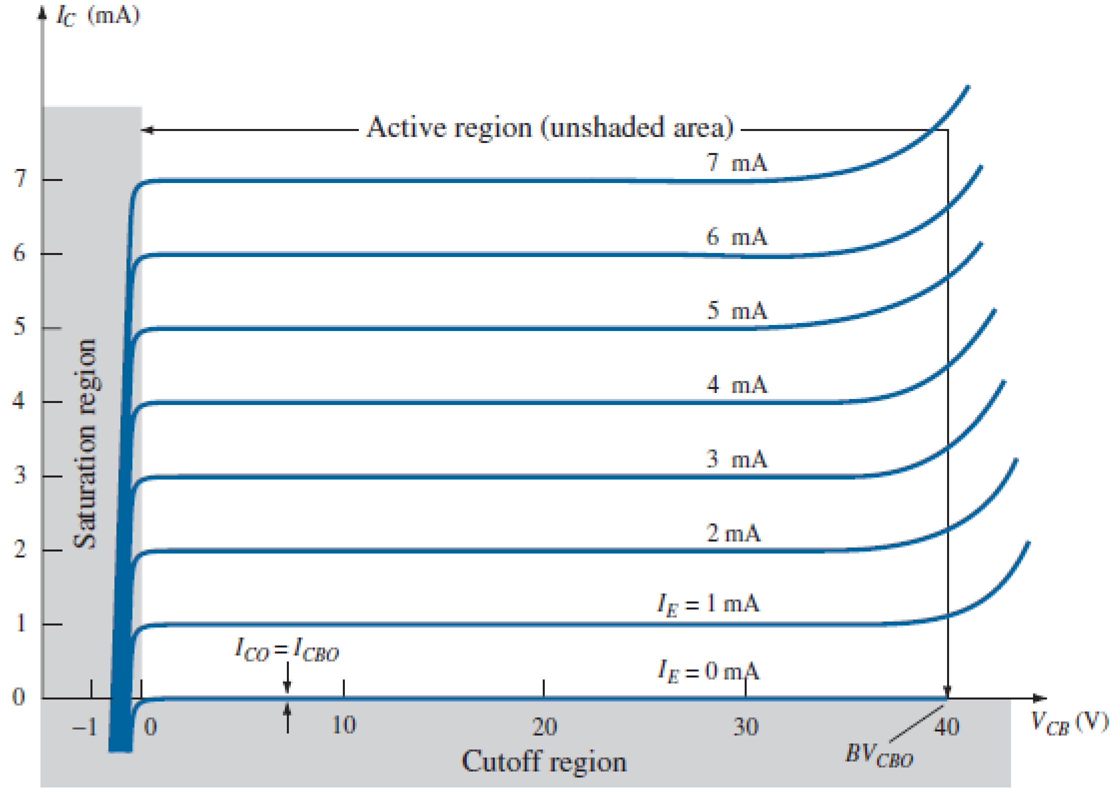


FIG. 8

Operating Regions

- **Active** – Operating range of the amplifier. It is noticed that IE is approximately equal to IC (IC≈ IE).
- **Cutoff** – the region where the collector current is approximately 0A (IC=ICBO). The amplifier is basically off. There is voltage, but little current
- **Saturation** – Region to the left of VCB=0. Note the exponential increase in collector current as the voltage VCB increases toward 0 V. There is current but little voltage.

- Approximations
- Emitter and collector currents:

$$\boxed{I_C \cong I_E}$$

- Base-emitter voltage:
- VBE = 0.7 V (for Silicon)

Alpha (a)

- **DC Mode** In the dc mode the levels of I_C and I_E due to the majority carriers are related by $$\alpha_{dc} = \frac{I_C}{I_E} \quad (3.5)$$ $$I_C = I_{C_{majority}} + I_{CO_{minority}} \quad (3.2)$$

where IC and IE are the levels of current at the point of operation. Even though the characteristics of Fig. 3.8 would suggest that α = 1, for practical devices alpha typically extends from 0.90 to 0.998, with most values approaching the high end of the range. Since alpha is defined solely for the majority carriers, Eq. (3.2) becomes $$I_C = \alpha I_E + I_{CBO} \quad (3.6)$$

- AC Mode For ac situations where the point of operation moves on the characteristic curve, an ac alpha is defined by $$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}} \quad (3.7)$$

EXAMPLE 3.1

a. Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 3$ mA and $V_{CB} = 10$ V.
b. Using the characteristics of Fig. 3.8, determine the resulting collector current if I_E remains at 3 mA but V_{CB} is reduced to 2 V.
c. Using the characteristics of Figs. 3.7 and 3.8, determine V_{BE} if $I_C = 4$ mA and $V_{CB} = 20$ V.
d. Repeat part (c) using the characteristics of Figs. 3.8 and 3.10c.

Solution:

a. The characteristics clearly indicate that $I_C \cong I_E = 3$ **mA.**
b. The effect of changing V_{CB} is negligible and I_C continues to be **3 mA**.
c. From Fig. 3.8, $I_E \cong I_C = 4$ mA. On Fig. 3.7 the resulting level of V_{BE} is about **0.74 V**.
d. Again from Fig. 3.8, $I_E \cong I_C = 4$ mA. However, on Fig. 3.10c, V_{BE} is **0.7 V** for any level of emitter current.

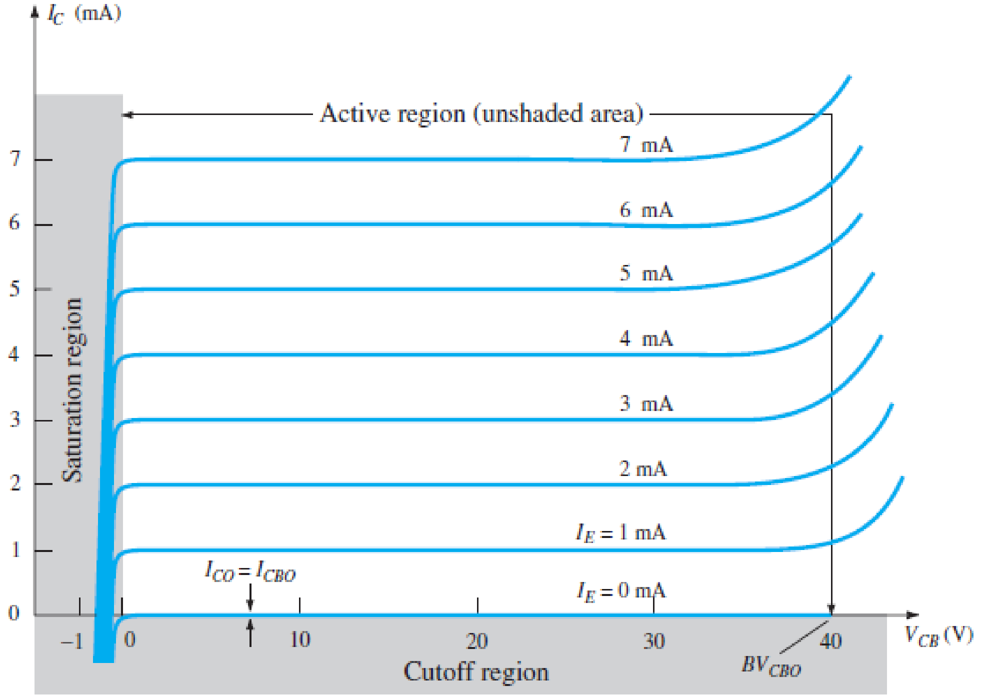


FIG. 3.8

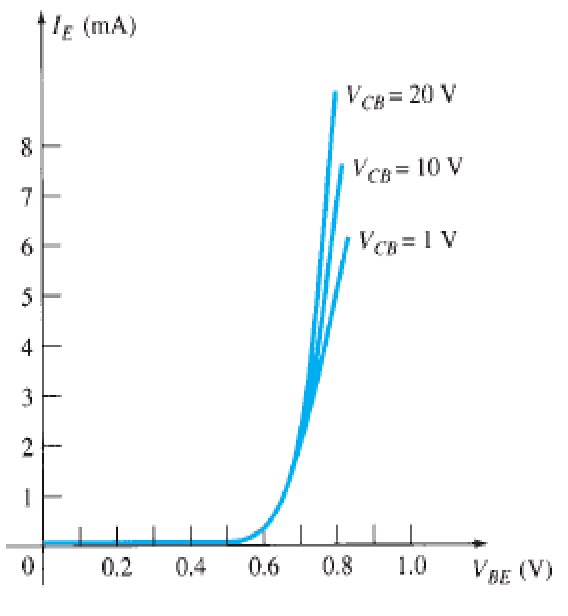


FIG. 3.7

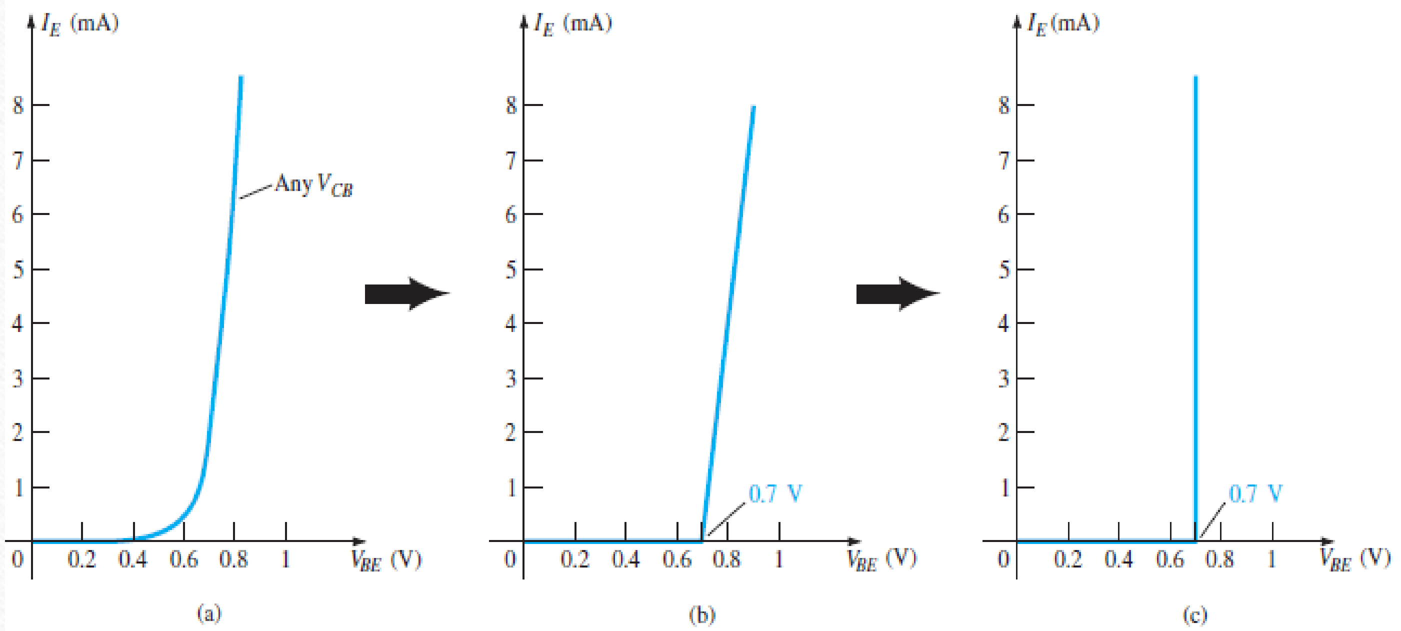


FIG. 3.10

Breakdown Region

- As the applied voltage VCB increases there is a point where the curves take a dramatic upswing in Fig. 3.8 As stated earlier the base-to-collector junction is reversed biased in the active region, but there is a point where too large a reverse-bias voltage will lead to the avalanche effect. The result is a large increase in current for small increases in the base-to-collector voltage.

Biasing

- The proper biasing of the common-base configuration in the active region can be determined quickly using the approximation $IC = IE$ and assuming for the moment that $IB =$ 0 mA. The result is the configuration of Fig. 3.11 for the *pnp* transistor. The arrow of the symbol defines the direction of conventional flow for IE IC. The dc supplies are then inserted with a polarity that will support the resulting current direction. For the *npn* transistor the polarities will be reversed.

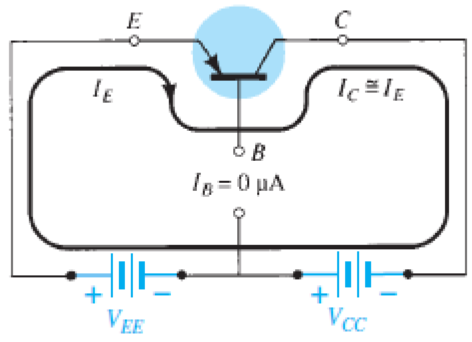


FIG. 3.11
Establishing the proper biasing management for a common-base pnp transistor in the active region.

COMMON-EMITTER CONFIGURATION

- The most frequently encountered transistor configuration appears in Fig. 3.12 for the *pnp* and *npn* transistors. It is called the *common-emitter configuration* because the emitter is common to both the input and output terminals (in this case common to both the base and collector terminals).

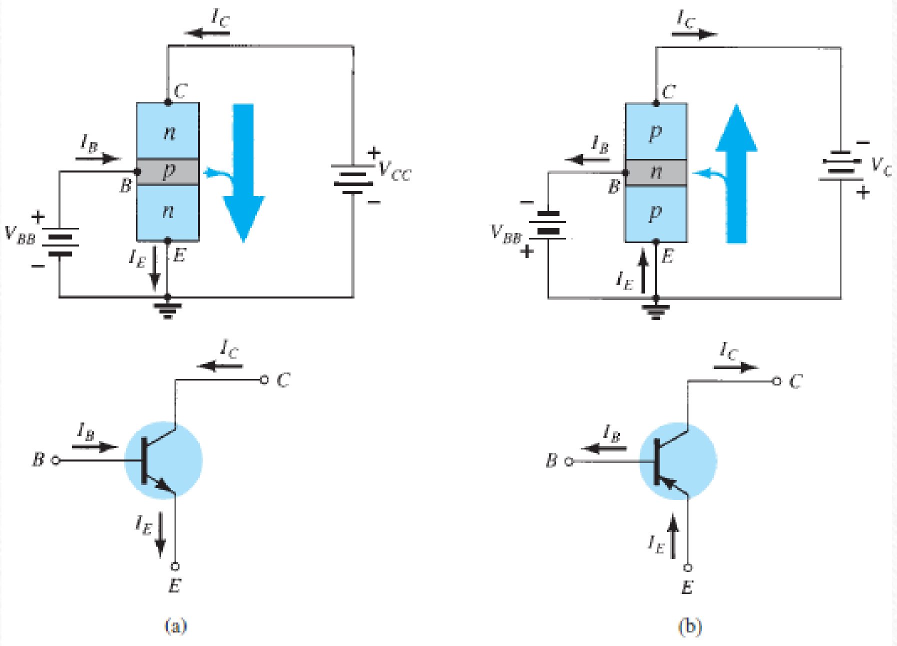


FIG. 3.12

- Two sets of characteristics are again necessary to describe fully the behaviour of the common-emitter configuration: one for the input or base–emitter circuit and one for the output or collector–emitter circuit. Both are shown in Fig. 3.13 .

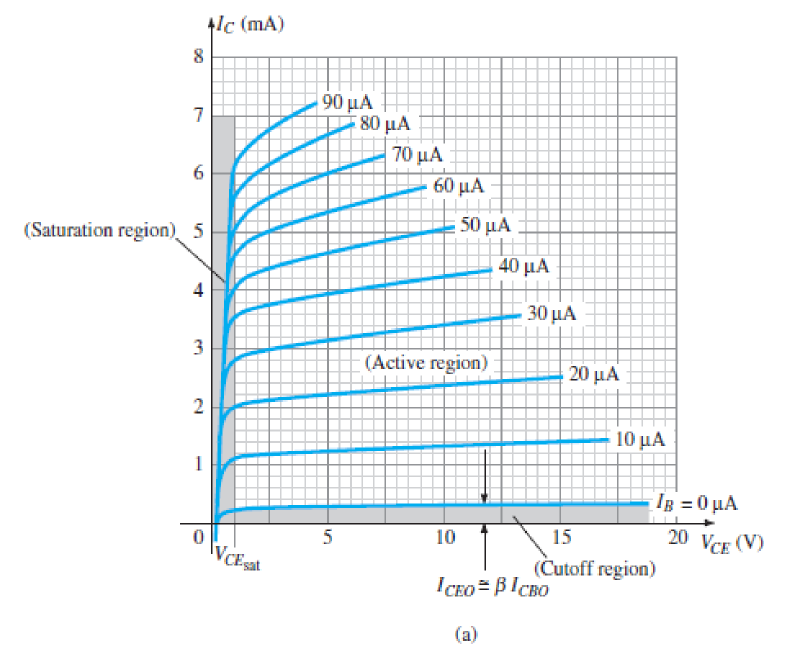


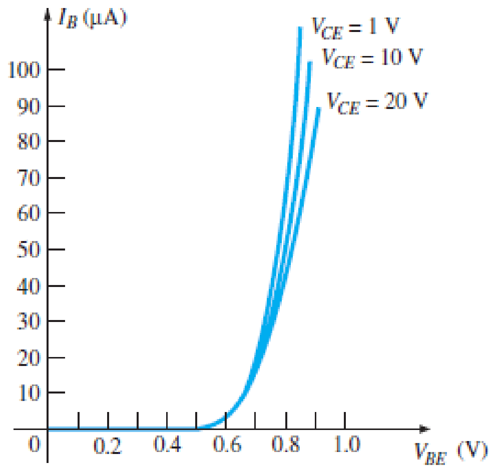
FIG. 3.13

EXAMPLE 3.2

a. Using the characteristics of Fig. 3.13, determine I_C at $I_B = 30\ \mu A$ and $V_{CE} = 10\ V$.
b. Using the characteristics of Fig. 3.13, determine I_C at $V_{BE} = 0.7\ V$ and $V_{CE} = 15\ V$.

Solution:

a. At the intersection of $I_B = 30\ \mu A$ and $V_{CE} = 10\ V$, $I_C =$ **3.4 mA**.
b. Using Fig. 3.13b, we obtain $I_B = 20\ \mu A$ at the intersection of $V_{BE} = 0.7\ V$ and $V_{CE} = 15\ V$ (between $V_{CE} = 10\ V$ and 20 V). From Fig. 3.13a we find that $I_C =$ **2.5 mA** at the intersection of $I_B = 20\ \mu A$ and $V_{CE} = 15\ V$.



(b)

Beta (β)

- DC Mode In the dc mode the levels of I C and I B are related by a quantity called beta and defined by the following equation:

$$\beta_{dc} = \frac{I_C}{I_B} \qquad (3.10)$$

- where IC and I*B* are determined at a particular operating point on the characteristics. For practical devices the level of β typically ranges from about 50 to over 400, with most in the midrange. As for a, the parameter b reveals the relative magnitude of one current with respect to the other. For a device with a b of 200, the collector current is 200 times the magnitude of the base current.
- AC Mode For ac situations an ac beta is defined as follows:

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} \qquad (3.11)$$

- The use of Eq. (3.11) in Fig. 3.17 . I B = 25 µA and V CE= 7.5 V as indicated on Fig. 3.16 . The restriction of V CE = 7.5 V

- by choosing two points on either side of the Q -point along the vertical axis I B = 20 µA and 30 µA

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}} = \frac{3.2\text{ mA} - 2.2\text{ mA}}{30\ \mu\text{A} - 20\ \mu\text{A}} = \frac{1\text{ mA}}{10\ \mu\text{A}} = 100$$

- If we determine the dc beta at the Q -point, we obtain $\beta_{dc} = \frac{I_C}{I_B} = \frac{2.7\text{ mA}}{25\ \mu\text{A}} = 108$

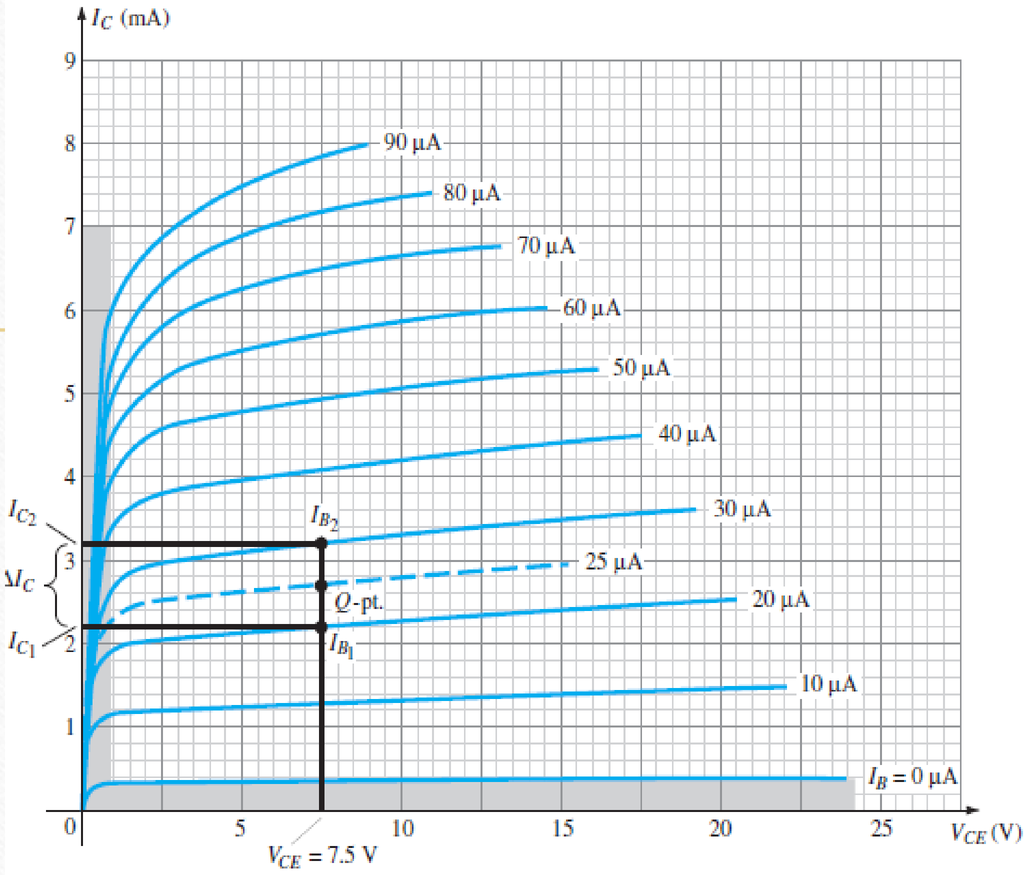


FIG. 3.16

Determining β_{ac} and β_{dc} from the collector characteristics.

- If the characteristics of a transistor are approximated by those appearing in Fig. 3.17 ,
- in I B is fixed at 10 μA and the vertical spacing between curves is the same at every point in
- the characteristics—namely, 2 mA. Calculating the β ac at the Q -point indicated results in

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\bigg|_{V_{CE}=\text{constant}} = \frac{9\text{ mA} - 7\text{ mA}}{45\ \mu\text{A} - 35\ \mu\text{A}} = \frac{2\text{ mA}}{10\ \mu\text{A}} = \mathbf{200}$$

- Determining the dc beta at the same Q -point results in $\beta_{dc} = \frac{I_C}{I_B} = \frac{8\text{ mA}}{40\ \mu\text{A}} = \mathbf{200}$

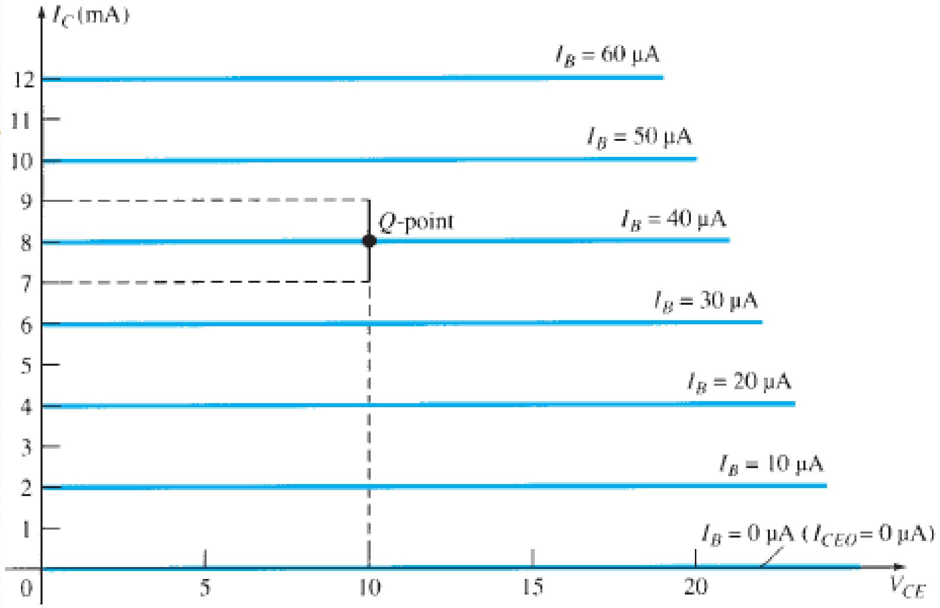


FIG. 3.17
Characteristics in which β_{ac} is the same everywhere and $\beta_{ac} = \beta_{dc}$.

- A relationship can be developed between β and α using the basic relationships introduced
- thus far. Using β= IC/IB, we have IB = IC/β, and from α = IC/IE we have
- IE = IC/α. Substituting into
- IE = IC + IB $\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$ dividing by Ic = $\frac{1}{\alpha} = 1 + \frac{1}{\beta}$

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

$$\boxed{\alpha = \frac{\beta}{\beta + 1}} \qquad (3.12)$$

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}} \qquad (3.13)$$

$$\boxed{I_C = \beta I_B} \qquad (3.15)$$

$$I_E = I_C + I_B$$

$$= \beta I_B + I_B$$

$$\boxed{I_E = (\beta + 1)I_B} \qquad (3.16)$$

Biasing

- Let us assume that we are presented with an npn transistor such as shown in Fig. 3.18a and asked to apply the proper biasing to place the device in the active region.
- IC + IB = IE. both IC and IB must enter the transistor structure

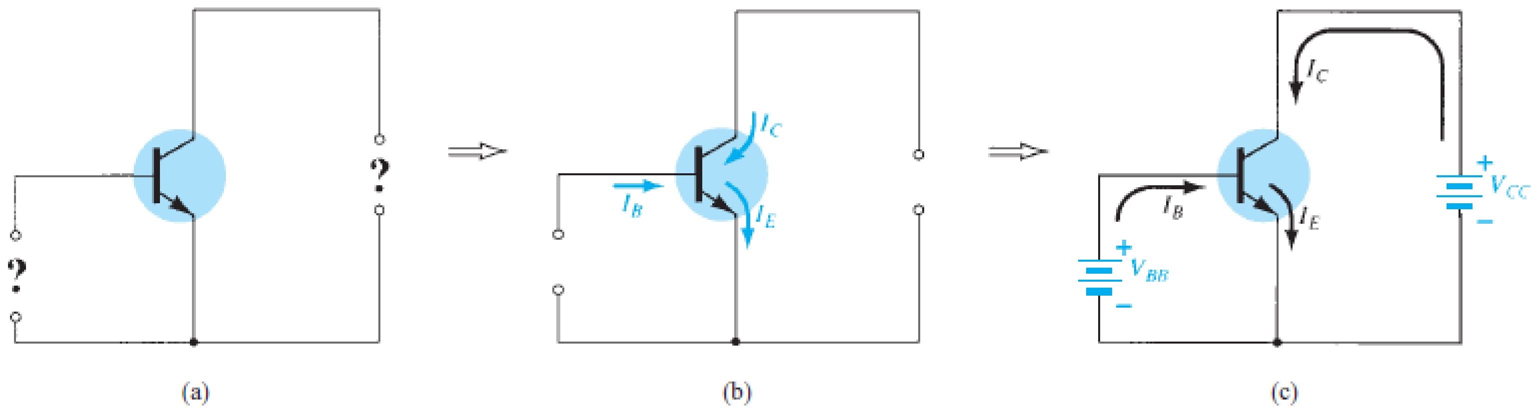


FIG. 3.18

COMMON-COLLECTOR CONFIGURATION

- The third and final transistor configuration is the common-collector configuration , shown in Fig. 3.20 with the proper current directions and voltage notation.
- It can be designed using the common-emitter characteristics
- For the common-collector configuration the output characteristics are a plot of IE versus VCE for a range of values of IB .

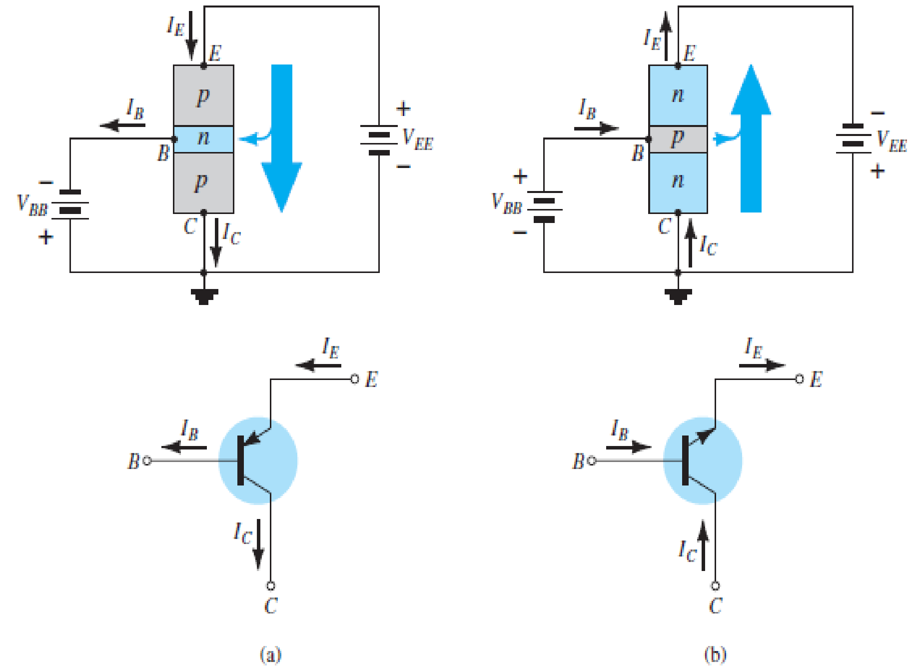


FIG. 3.20
Notation and symbols used with the common-collector configuration: (a) pnp transistor; (b) npn transistor.

LIMITS OF OPERATION

- For each transistor there is a region of operation on the characteristics that will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion. Such a region has been defined for the transistor characteristics of Fig. 3.22 .
- The maximum dissipation level is defined by the following equation:

$$\boxed{P_{C_{max}} = V_{CE} I_C} \qquad (3.17)$$

- If the characteristic curves are unavailable or do not appear on the specification sheet (as is often the case), one must simply be sure that IC , VCE , and their product V CE IC fall into the following range:

$$I_{CEO} \leqq I_C \leqq I_{C_{max}}$$
$$V_{CE_{sat}} \leqq V_{CE} \leqq V_{CE_{max}} \qquad (3.18)$$
$$V_{CE}I_C \leqq P_{C_{max}}$$

- For the common-base characteristics the maximum power curve is defined by

$$P_{C_{max}} = V_{CB}I_C \qquad (3.19)$$

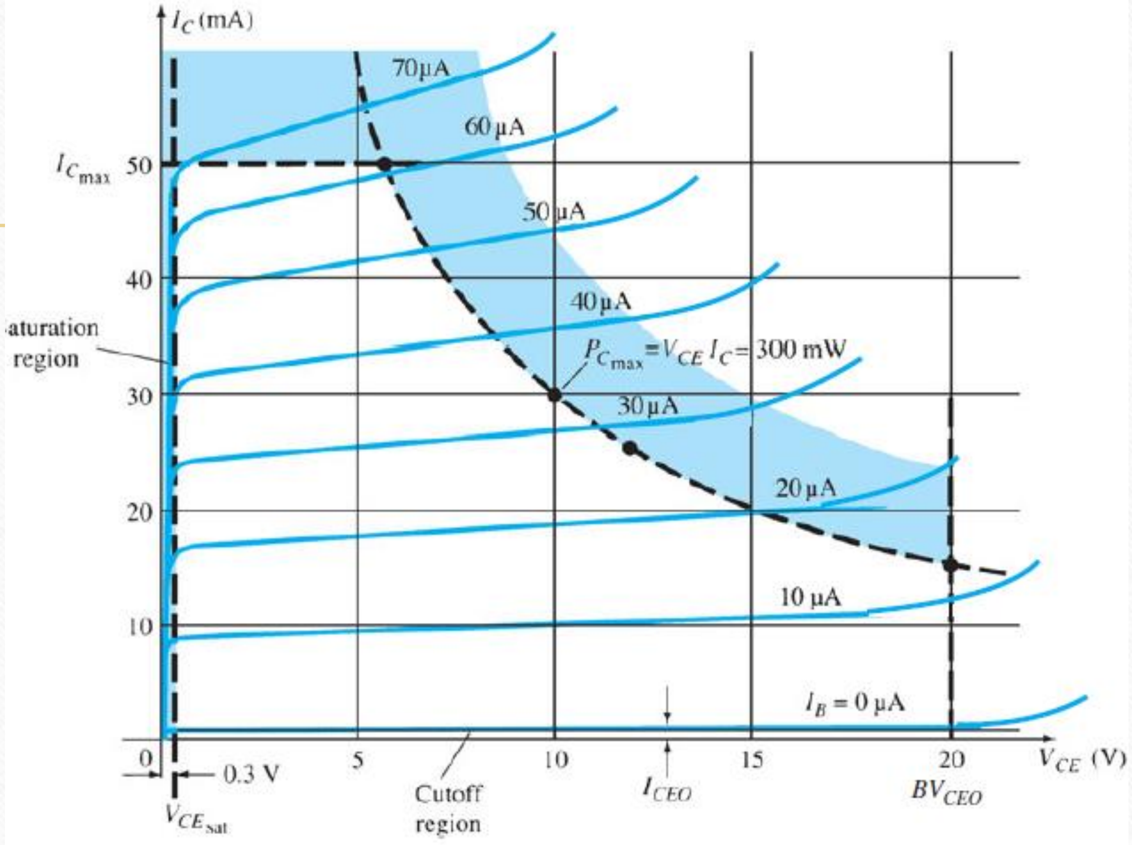


FIG. 3.22

Thank you for your attention